[This question paper contains 2 printed pages.]

Sr. No. of Question Paper : 2052 **Your Roll No.....**

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Unique Paper Code: 2512011202
Name of the Paper: Digital Electronics
Name of the Course: B.Sc(H) Electronics (Core)
Semester: II (Under NEP UGCF mode)
Duration: 03 Hour
Maximum Marks: 90

Instruction for Candidates

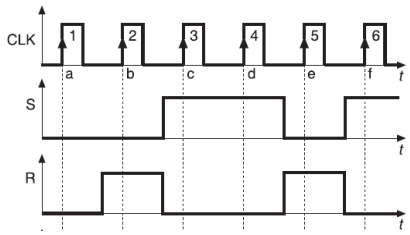
1. Write your Roll No. on the top immediately on receipt of this question paper.
2. Attempt any 5 questions in all, including question 1 which is compulsory.
3. Use of Scientific Calculator is allowed.

Q1 (a) Convert $(230.3)_{10} = (\ )_2 = (\ )_8 = (\ )_{16}$ (3)

(b) Simplify the expression using Boolean Algebra. (3)
Y= [(XY' + XYZ)' + X(Y+XY')]

(c) 1101010 is a signed binary number. Determine its decimal value in (i) sign magnitude form and (ii) 2s complement form. (3)

(d) The waveforms as shown in the figure below are applied to the edge-triggered S-R flip-flop. Draw the output waveform. (3)



(e) What are PRESET and CLEAR inputs? (3)

(f) Define the following: (3)
(i) Fan-in
(ii) Fan-out
(iii) Noise Margin

Q2 (a) Prove that (6)
(i)$AB + (AC)' + AB'C(AB + C) = 1$
(ii) If $A + B = A + C$ and $A' + B = A' + C, then\ B = C$
(iii) Without reducing convert the following expression into NAND logic $(1 + A)(AC)$

(b) Perform the following using binary multiplication and computer method of multiplication (6)
$(1001)_2 \times (1101)_2$

(c) Detect and correct errors in the following even parity Hamming code words (6)
(i)1101010
(ii) 0111101

Q3 (a) Minimize the expression using K-maps and implement it using NAND-NAND logic (6)
$Y = \prod M(0,1,3,5,6,7,10,14,15)$

(b) Design a combinational logic circuit with 4 input variables that will produce logic 1 output when the number of 1s in the output is even. (6)

(c) Implement the given function using 8x1 Multiplexer. (6)
$F = \sum m(0,1,3,4,6,8,10,11,12,15)$

Q4 (a) Draw the circuit of a BCD adder and explain its working. (6)

(b) Implement given expressions using a decoder (6)
$Y1 = \sum m(0,2,6,8,10)$
$Y2 = \sum m(4,5,6,8)$
$Y3 = \sum m(10,11,13)$
$Y4 = \sum m(6,7,9,11,15)$

(c) Use tabular method to minimize the expression (6)
$F = \sum m(0,2,3,6,7,8,9,10,13)$

Q5 (a) Convert a SR flip-flop into a T flip-flop. Derive the required input equations using excitation and characteristic tables and draw the logic circuit diagram. (6)

(b) Why are edge-triggered flip-flops preferred over level-triggered flip-flops? Explain the problem of race-condition in JK flip flop and how it can be eliminated. (6)

(c) Design a type D counter that goes through states 0, 1, 2, 4, 0, … . The unused states must always go to zero (000) on the next clock pulse. (6)

Q6 (a) Draw the logic diagram of 4 bit serial in serial out shift register and explain its working with an example. (6)

(b) Design a synchronous MOD-10 (Decade) counter using T flip-flop. Show how the counter resets automatically. (6)

(c) Obtain the excitation table, state table and state diagram representing the operation of a D flip-flop. Also, write its characteristic equation based on the state table. (6)

Q7 (a) Explain the working principle of a Successive Approximation ADC with diagram. (6)

(b) What is the difference between ROM and RAM. Mention any three different types of ROM and explain their working. (6)

(c) Show how the FPLA can be programmed to implement a full subtractor. (6)