(This Question paper contains 2 printed page)

Your Roll No……

Sr. No. of Question Paper : 1792

Unique Paper code: 2512041201
Name of the paper: Fundamentals of Digital Circuits
Name of course: B.Sc(H) Instrumentation (Core)
Semester: II
Duration: 3Hours
Maximum Marks: 90

Instructions for Candidates:

1. **Use of scientific calculator is allowed.**
2. **Question No.1 is compulsory. All questions carry equal marks. Attempt any 5 questions in all.**

Q.1	(a)	Differentiate between sequential and combinational logic circuits	(3)
	(b)	Define Figure of Merit and Fan Out of Logic Families.	(3)
	(c)	Distinguish between synchronous and asynchronous counters	(3)
	(d)	Find the characteristic equation of SR flip-flop.	(3)
	(e)	Check whether $A \cdot C + A \cdot B \cdot C = A \cdot C$ is true or false?	(3)
	(f)	What is the minimum number of flip-flops needed to build a counter of modulus 60?	(3)
Q.2	(a)	Convert $(675.625)_{16}$ into Hexadecimal and Octal number system	(6)
	(b)	Solve the following: i) $(1101)_2 - (111)_2 = (?)_2$ ii) $(4C)_{16} + (3A)_{16} = (?)_{16}$ iii) $(111)_2 * (101)_2 = (?)_2$	(6)
	(c)	Use a truth table to prove that $x \cdot (y+z) = (x \cdot y) + (x \cdot z)$	(6)
Q.3	(a)	Write the truth table and draw the circuit of a Full Adder.	(6)
	(b)	Design a combinational logic circuit that has four inputs A, B, C, D. The output should be high, when any two inputs are high.	(6)
	(c)	What is the equivalent Product of Sum (POS) expression for the Boolean expression x'y'z + yz + xz? Also draw AOI logic circuit diagram of the given expression.	(6)
Q.4	(a)	Design the function $F(A,B,C) = \Sigma(1,2,5,7)$ using a 4 to 1 MUX	(6)
	(b)	Implement a full subtractor using 3 to 8 line decoder and logic gates.	(6)
	(c)	Design a MOD-10 synchronous up counter using D Flip Flop.	(6)
Q.5	(a)	Draw the circuit diagram and timing diagram of a MOD-6 ripple counter using negative edge triggered T flip flop.	(8)
	(b)	Design a 3 bit gray to binary code converter.	(6)
	(c)	Differentiate between PLA and PAL.	(4)
Q.6	(a)	Draw the logic diagram for a 4-bit Ring counter. Also Draw the timing diagram and the sequence. Assume initial state to be 0001.	(8)
	(b)	Give the circuit diagram of totem pole output of TTL NAND gate and explain its	(6)

functioning.

(c) Use 2's complement subtraction to subtract $(27)_{10}$ from $(75)_{10.}$ (4)

Q.7 (a) Draw and explain the circuit of a 3-bit parallel-in-serial-out (PISO) shift register (6)

(b) Using K-map, obtain simplified POS expressions for the following functions: (6)

$F(A,B,C,D) = \Sigma m(0,1,2,3,4,5) + d(10,11,12,13,14,15)$

(c) Convert SR Flip Flop to D Flip Flop using excitation table. (6)