(This Question paper contains 2 printed pages) Roll No. _____

S.No. of Question Paper : 7974
Unique Paper Code : 2513010021
Name of the Course : B.Sc.(H) Electronics (GE)
Name of the Paper : CMOS Digital VLSI Design
Semester : VII
Duration : 3 hours
Maximum Marks : 90

Instruction for Candidates

1. There are seven questions in all, out of which attempt any five questions.
2. All questions carry equal marks.
3. First Question is Compulsory.

Q1 a) What are the key differences in VHDL and Verilog?
b) What are the main parts of a VHDL code.
c) Write a short code for a two input AND gate with delay of 5 units in Verilog.
d) What are four basic values of Verilog value set?
e) Why is refresh circuitry needed in a DRAM cell?
f) What is LVS and parameter extraction in VLSI? 3x6

Q2 a) Compare the three types of modelling in VHDL. Discuss briefly with examples. 6
b) Write a code in VHDL to implement Full Adder. 7
c) Describe the various data objects in VHDL. 5

Q3 a) Compare the statements 'WHEN ELSE' and 'WITH WHEN SELECT' with the help of an example. 6
b) Discuss with the help of an example, the role of components and port mapping in Structural Modelling in VHDL. 7
c) Briefly explain the various relational and logical operators in VHDL. 5

Q4 a) What will be the execution sequence and output of statements in the code of a stimulus block given below:

```
module stimulus;
reg x,y,a,b,m;
initial
      m=1'b0;
initial
begin
      #5 a=1'b1;
      #25 b=1'b0;
end
initial
begin
      #10 x=1'b0;
      #25 y=1'b1;
end
initial
      #50  $finish;
endmodule
```

6
b) Write a Verilog code for 4X1 MUX using gate level modelling. 7
c) Describe Port connection rules in Verilog. 5

Q5 a) How conditional operators can be used in Verilog for behavioural modelling. Explain with example. 7

b) Briefly describe hierarchy and the four levels of abstraction in Verilog. 6

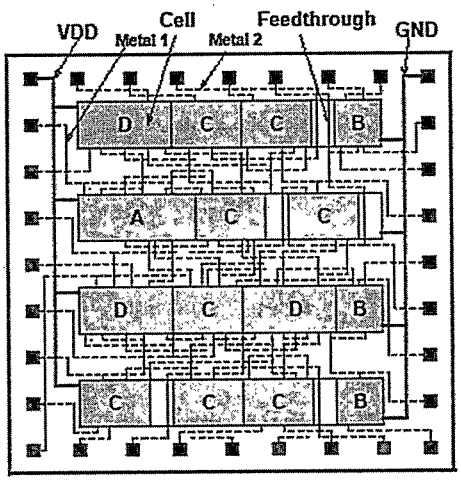
c) When we have many alternatives to choose which one is better using nested if-else-if or case statement in Verilog? Explain with examples. 5

Q6 a) What are the advantages and disadvantages of a 6T full CMOS SRAM? 6

b) What is access time penalty in 6T Full CMOS SRAM cell and how is it reduced? 5

c) Draw and explain the typical voltage waveforms associated with 3-T DRAM cell during four consecutive operations: write "1," read "1," write "0," and read "0." 7

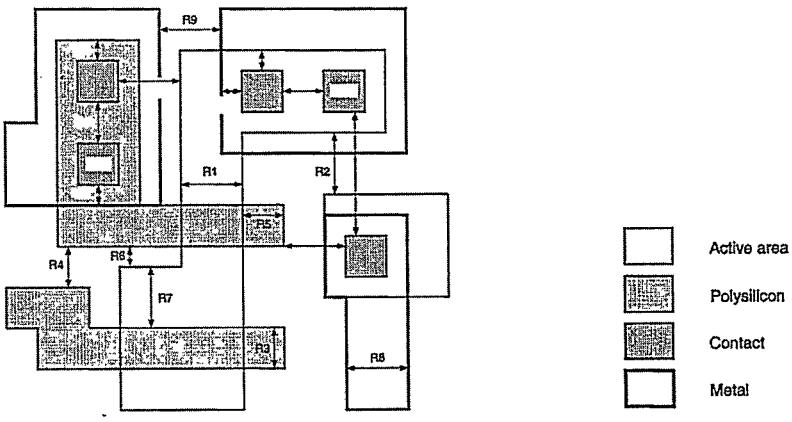
Q7 a)



Based on the given layout diagram, What is the CMOS VLSI design methodology used? What does A,B,C and D signify? Explain the function of each labelled component. 6

b) What are the various steps involved in the ASIC Design Flow? Elaborate on Front-end and Back-end design. 6

c)



Identify the regions from R1 to R9 and provide their typical value based on the λ based scaling design rules 6