[This question paper contains 2 printed pages.]

Your Roll No.....

L

Sr. No. of Question Paper : 7296

Unique Paper Code : 2513010021 / 25130100 21

Name of the Paper : CMOS Digital VLSI Design

Name of the Course : **B.Sc. (H) Electronics (GE)**

Semester : VIII

Duration : 3 Hours Maximum Marks : 90

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. There are **seven** questions in all, out of which attempt any **five** questions.
3. **All** questions carry equal marks.
4. **First** Question is Compulsory.

Q1 a) In what situations is the 'always' statement used in Verilog?

b) Using Keyword "XOR" in VHDL and Verilog is same or different. Explain.

c) Differentiate between 'signal' and 'variable' in VHDL.

d) Discuss the various data types used in Verilog.

e) Explain read stability in 6T SRAM Explain with relevant diagram.

f) What is the need for design rules? Mention and explain any two layout design rules specification methods. 3x6

Q2 a) Write a VHDL code to implement a 2 to 4 decoder. 7

b) Explain structural modelling in VHDL with the help of an example. 6

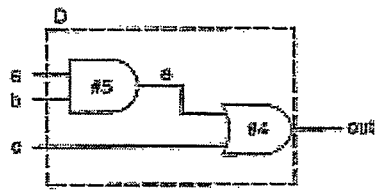
c) What are various types of operators available in VHDL. Describe each type with the help of an example. 5

Q3 a) VHDL is a concurrent language, explain? What instructions are used to write a sequential code? 5

b) Write a VHDL code that sends an output signal to an LED based on a 2-input mode m:
m=00, turn LED off
m=01, turn LED on
m=10, toggle LED
m=11, unchanged 7

c) What are the different data types in VHDL? List various rules to write an identifier. 6

Q4 a) Module D is defined by the circuit:



The stimulus block for the above circuit is given as

```
module stimulus;
reg a, b, c;
wire out;
D d1(out, a, b, c);
initial
```

7

P.T.O.

```
begin
    a=1'b0; b=1'b0; c=1'b0;
    #10 a=1'b1; b=1'b1; c=1'b1;
    #10 a=1'b1; b=1'b0; c=1'b0;
    #20 $finish;
end
endmodule
```

Draw the waveforms for a,b,c,e and out for the given simulation.

b) Differentiate between blocking and non-blocking statements using examples in Verilog. 5

c) In a 4X1 multiplexer design, the concatenation operator enables the use of two selection lines as a single entity. Write a Verilog code for this implementation. 6

Q5 a) Write a code in Verilog to implement full adder using gate level modelling. 7

b) What is the difference between connecting ports by name and connecting ports by order. Explain with example. 6

c) What are different loops available in Verilog. Explain. 5

Q6 a) Give a comparison between 4T *Resistive-load* SRAM cell and 6T Full CMOS SRAM cell. 6

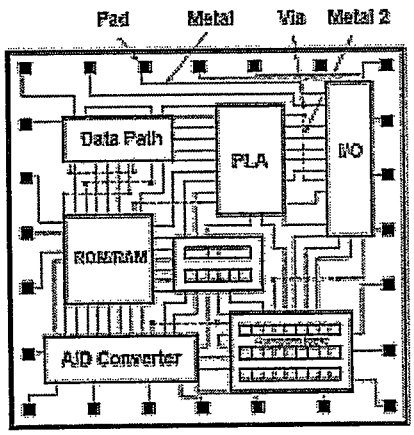
b) Draw and explain the typical voltage waveforms associated with the 6-T full CMOS SRAM cell during four consecutive operations: write "1," read "1," write "0," and read "0." 7

c) Explain the Open and Folded bitlines in DRAM. 3

Q7 a) Draw a properly labelled standard cell layout design for a CMOS inverter. 6

b) What are the various steps involved in the FPGA Design Flow? Elaborate on Front-end and Back-end design. 6

c)



Identify the CMOS VLSI design methodology applied in the given layout diagram. Describe the function of each labelled component. 6