[This question paper contains 2 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 9496 **K**

Unique Paper Code : 2513040021

Name of the Paper : CMOS Digital Integrated Circuit Design

Name of the Course : **B.Sc. (H) Instrumentation (DSE)**

Semester : VII

Duration : 3 Hours Maximum Marks : 90

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. There are **seven** questions in all, out of which you have to attempt any **five** questions.
3. Question No. 1 is compulsory.
4. All questions carry equal marks.
5. Use of Non-programmable Scientific calculator is allowed

Q.1 (a) Explain operation of Complementary MOS inverter in the transition region (3)

(b) Explain the working principle of a CMOS transmission gate. Why is it preferred over a single NMOS or PMOS switch? (3)

(c) Define a sequential circuit. How does it differ from a combinational circuit in CMOS logic design? (3)

(d) What is the difference between volatile and non-volatile memory? Give one example of each. (3)

(e) In a CMOS inverter, if the voltage transfer characteristic has V_{IH} = 3V and V_{IL} = 1V, calculate the noise margins N_{MH} and N_{ML} given V_{DD} = 5V (assume $V_{OH} \approx V_{DD}$ and $V_{OL} \approx 0V$). (3)

(f) If a processor has a 64K × 8-bit memory, how many address lines are required? (3)

Q.2 (a) Draw and explain the Voltage Transfer Characteristics (VTC) of a CMOS inverter. (8)

(b) Discuss calculation of gain of a CMOS inverter from its voltage transfer characteristics. Derive an expression for $\frac{dV_{out}}{dV_{in}}$ and explain its significance near the threshold point. (6)

(c) Describe the static behavior of a CMOS inverter when the input voltage transitions from low to high. (4)

Q.3 (a) Implement the following Boolean function using Complementary MOS logic. (6)

$$Y = \overline{(D + E + A)(B + C)}$$

P.T.O.

(b) Describe the design and operation of CMOS NOR gate. Discuss its pull-up network configurations. (6)

(c) Implement a 2 X 1 Multiplexer using Transmission gates and interpret its operation using different input combinations (6)

Q.4 (a) Realize Edge triggered D-Flip-Flop using Transmission gates and explain its operation. (6)

(b) Draw diagram and explain the implementation of SR latch using Complementary MOS NOR gates. (6)

(c) Explain the working of a CMOS clocked flip-flop circuit. Compare its operation for positive and negative edge triggering. (6)

Q.5 (a) Discuss memory classification using a diagram. Explain hierarchical organization from registers to secondary storage. (6)

(b) Describe the internal structure and working of a ROM cell array. Explain how data is read and the significance of address decoding. (6)

(c) List different types of RAM cells. Draw and explain the operation of a single bit dynamic RAM cell. (6)

Q.6 (a) Write the logic equation for a 1-bit CMOS full adder and derive the output expressions for Sum and Carry. (6)

(b) Differentiate between SRAM and DRAM based on cell structure and data retention method. (6)

(c) Explain the concept of charge storage and charge leakage associated with pass transistor logic. (6)

Q.7 (a) Design a XOR gate using Transmission gate Logic. (6)

(b) Derive the expression for the switching threshold (V_M) of a CMOS inverter. (6)

(c) Differentiate between Dynamic CMOS and Static CMOS. (6)