3	001
4	011
5	111
6	110
7	001

c. Explain how the physical defects can be realised as electrical and logical faults in the circuits. (6)

[This question paper contains 8 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 5843 **K**

Unique Paper Code : 2512013503

Name of the Paper : Basic VLSI Design

Name of the Course : B.Sc. (H) Electronics (DSC)

Semester : V (Under NEP UGCF Mode)

Duration : 3 Hours Maximum Marks : 90

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. There are **Seven** questions in all, out of which you have to attempt **any one** questions.
3. All questions carry equal marks
4. Use of non-programmable Scientific Calculator is allowed
5. First Question is Compulsory.

1. a) Draw the output characteristics of MOSFET. Define Triode, Deep Triode and Saturation regions. (3)

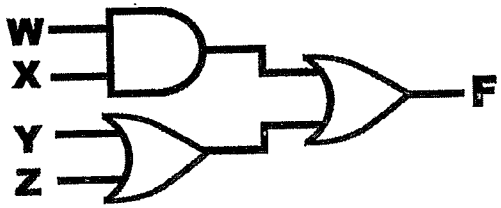
b. For a PSPICE model having following instruction: (3)

M1 2 1 0 0 NMOS1

Explain the significance of each term.

c. Calculate the noise margins of a CMOS inverter given V_{OL}=0.1V, V_{OH}=4.9V, V_{IL}=1.0V and V_{IH}=2.0 V. (3)

d. Define rise time, fall time and time period of a dynamic waveform. (3)



7. a. Explain the construction of the one-transistor DRAM cell. Also explain the various operations of the DRAM Cell (6)

b. Design a n-MOSFET programmable ROM that contains the following data: (6)

Address	Data
0	100
1	111
2	010

b. Using any two input logic gate design, explain the merits and demerits of pass transistor logic over CMOS logic circuitry. (6)

c. Sketch the CMOS circuit diagram to implement function, $F=\overline{(A\bullet B)+(C\bullet D)}$ (6)

6. a. Draw two-input XOR gate using CMOS logic and explain its working for different truth table input conditions. Also, explain why it is referred to as non-equivalence checker circuit (6)

b. Explain the concept of overlapping clocks in dynamic transmission gate master slave edge triggered register. (6)

c. Consider the logic shown in the diagram and draw the CMOS based circuit for the function F (6)

e. In static CMOS logic circuit design, why PMOS logic array and NMOS logic array are referred to as Pull-Up Network (PUN) and Pull-Down Network (PDN)? (3)

f. What is scan based techniques? 3 2. (3)

2. a. Considering gradual channel approximation derive the expression for Drain current equation of the MOSFET having the effective channel length 'L'. (6)

b. What is 'Pinch-off' condition in MOSFET. Explain how it can be achieved. What will happen if drain to source voltage is increased after the channel is pinched off. (6)

c. For a particular IC fabrication process, the

transconductance parameter $K'_n = 50\mu A/V^2$, and V_{TH}=1V. In an application in which V_{GS}=V_{DS}=5V, a drain current of 0.8mA is required of a device of minimum length of 2μm. What value of channel width must the design use? (6)

3. a. What is process technology parameter? How it is related to Channel Length Modulation? Determine the expression for output conductance and show it strongly depends on channel length. (6)

b. What are interface Traps. Derive the expression for Threshold voltage, showing the sign of various components of Threshold voltage for N-channel and P channel devices. (6)

c. A CMOS inverter operates at V_{DD} = 5 V, with Kn = 100 μA/V², Kp = 40 μA/V². Find the switching

threshold (VM). (6)

4. a. Explain the principle of operation of a CMOS inverter. Discuss the roles of the load and driver transistors and how the inverter performs logic inversion (6)

b. Derive the expression for critical voltages for a n-MOS inverter circuit with resistive load (6)

c. Estimate the power consumption of a CMOS inverter with load capacitance 5pF, operating at 100 MHz, and V_{DD} = 1.8 V (6)

5. a. Derive the expression for Noise Margins (NMH and NML) of a CMOS inverter in terms of the transfer characteristics (6)