(c) Write the micro-operations for the following instructions (6)

(i) ISZ

(ii) SPA

(iii) LDA

7. (a) Perform the arithmetic operation (-65) + (-85) with binary numbers in signed-2's complement representation. Use eight bits to accommodate each number together with its sign. Identify, if this operation results in overflow or not. (6)

(b) Differentiate between (9)

(i) RISC and CISC

(ii) Programmed I/O and Interrupt-initiated I/O

(iii) Burst transfer and Cycle stealing in DMA

[This question paper contains 8 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 5823 **K**

Unique Paper Code : 2342011102

Name of the Paper : Computer System Architecture

Name of the Course : **B.Sc. (H) Computer Science (NEP)**

Semester : I

Duration : 3 Hours Maximum Marks : 90

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. This question paper has **two** sections **A** and **B**.
3. **Section A** carries **30** marks and each question in **Section B** carries **15** marks.
4. Question **1** in **Section A** is compulsory.
5. Attempt any **4** questions from **Section B**.
6. Parts of a question must be attempted together.

Section A

1. (a) Perform the arithmetic operation $(-62)_{10} + (71)_{10}$ using 10's complement. (3)

(b) Write three differences between GPU and CPU. (3)

(c) Why do computer systems require an I/O interface? Give any three reasons. (3)

(d) Given the 8-bit binary number 0010 1101, perform a left shift (using CIL) by 2 positions.

(i) What is the resulting binary value?

(ii) What is the hexadecimal equivalent before and after shifting? (3)

(e) In the general register organization of a computer, a 14-bit control word includes the fields SELA, SELB, and SELD (each 3 bits) for register selection, along with the OPR field. Using this format, show how to implement the micro-operation

$$R2 \leftarrow R4 + R3,$$

given that the OPR code for addition is 00011 and register numbers are represented using their corresponding binary codes. (3)

6. (a) A processor executes one instruction in 80ns without pipelining. With pipelining, the processor is divided into 6 stages, each requiring 18ns.

(i) Find the total execution time for 200 instructions in both pipelined and non-pipelined processors.

(ii) Determine the speedup ratio of the pipelined processor. (4)

(b) A computer stores a two-word instruction starting at memory address 240. The address field of the instruction is located at 241, and it contains the value 180. The Program Counter (PC) holds 242 (address of the next instruction). The Index Register (XR) contains 25, and Register R2 contains 400. Determine the Effective Address (EA) for the instruction under the following addressing modes:

(i) Direct addressing

(ii) Immediate addressing

(iii) Relative addressing

(iv) Indexed addressing

(v) Register indirect addressing (5)

and the content of AC is A137. Go over the instruction cycle and determine the contents of the following registers at the end of the execute phase: PC, AR, DR, AC, and IR. (5)

(c) Convert the following : (6)

(i) $(C23)_{16}$ to octal

(ii) $(10101.010)_2$ to decimal

(iii) $(36.25)_{10}$ to octal

5. (a) What do you mean by Isolated I/O? Write its advantage and disadvantage. (4)

(b) Explain the interrupt cycle with the help of a flowchart. (5)

(c) Simplify the following Boolean function, F together with don't care conditions, d in sum-of-products form by means of a 4-variable K-map and draw the logic diagram of the simplified expression

$F(w,x,y,z) = \Sigma(1,2,6,7,8,13,14,15)$

$d(w,x,y,z) = \Sigma(0,3,5,12)$ (6)

(f) How many 8K × 8 RAM chips are needed to provide a memory capacity of 32K × 16 bits? (3)

(g) Using Boolean algebra, show that :

$AB + (AC)' + AB'C(AB+C) = 1$ (3)

(h) Explain decoder. Draw the block diagram of a 4×16 decoder using two 3×8 decoders. (3)

(i) Draw a space-time diagram for a five-segment pipeline showing the time it takes to process seven tasks. (3)

(j) Explain, with the help of a block diagram, how a D flip-flop can be constructed using a JK flip-flop. (3)

Section B

2. (a) A computer has a memory of 64K words, each 32 bits wide. One memory word 4 stores a single instruction. The instruction contains four fields: an addressing-mode field (to select one of 4 addressing modes), an opcode field, a register code (to select one of 30 registers), and an address field. Specify the number of bits required for the addressing-mode, opcode, register code, and address fields. (4)

P.T.O.

(b) What do you understand by cache memory? Compare main memory, auxiliary 5 memory and cache memory in terms of speed, cost and function. (5)

(c) Write the micro-operations for BSA instruction. If the instruction BSA 470, stored 6 at memory location 30 is executed, then answer the following:

(i) At which memory location will the return address be saved?

(ii) After saving the return address to which memory location will control transfer?

(iii) Which instruction is used at the end of the subroutine to return to the calling program?

(iv) What value will be loaded into the PC when the return instruction is executed? (6)

3. (a) Define the full adder with the help of truth table and logic diagram. Also, write Boolean expression for carry and sum operations. (4)

(b) Given the Boolean function (5)

$F = xy + xyz' + x' yz$

(i) List the truth table of function, F.

(ii) Draw the logic diagram of the original Boolean expression.

(iii) Simplify the algebraic expression using Boolean algebra.

(iv) Give the number of gates used in the simplified expression and the original expression.

(c) Explain 4-bit binary adder-subtractor with the help of diagram. If the adder-subtractor circuit has the values M=0, A=0111, B=0110 for input mode M and data inputs A and B, then determine the values of the outputs: S_3, S_2, S_1, S_0, and C_4. (6)

4. (a) Construct a 16-to-l-line multiplexer with two 8-to-l-line multiplexers and one 2-to-1-line multiplexer. Give the block diagram and the function table for the same. (4)

(b) An instruction stored at address 021 in the basic computer has I is equal to 0, an operation code of the AND instruction and an address part equal to 083 (all numbers are hexadecimal). The memory word at address 083 contains the operand B562