S.No. 9974

[This question paper contains 2 printed pages]

Unique Paper Code : 2513010021
Name of the Course : B.Sc.(H) Electronics
Name of the Paper : CMOS Digital VLSI Design
Semester : VII
Duration : 3 hours
Maximum Marks : 90

Instruction for Candidates

1. There are seven questions in all, out of which attempt any five questions.
2. All questions carry equal marks.
3. First Question is Compulsory.

Q1 a) Describe the basic structure of a VHDL program with the help of a neat block diagram.
b) What is concurrent signal assignment in VHDL?
c) How a rise time and fall time delays are specified for a gate in Verilog.
d) What is meant by blocking and non-blocking assignments.
e) Explain the refresh circuity for DRAM.
f) Why should the substrate be tied to Ground and N-Well to VDD in n-well CMOS process? What will be the situation for a p-well CMOS process and why? 3x6

Q2 a) Explain bit, std_logic, std_logic_vector, integer, boolean, and enumerated in VHDL. 6
b) Discuss 8X1 MUX in VHDL using WHEN ELSE statements. 7
c) What is difference between writing a code for combinational logic and sequential logic in VHDL. Explain with an example. 5

Q3 a) Write a code in VHDL to implement full subtractor using data flow modelling. 6
b) Explain with example, the structural modelling style in VHDL. 6
c) Explain arithmetic, logical, relational, shift, and concatenation operators with examples in VHDL 6

Q4 a) In Verilog if following statements are written inside module, then explain the result Y for all statements.

```
A = 1'b1, B = 2'b00, C = 2'b10, D = 3'b110;
Y = {B, C};
Y = {A, B, C, D, 3'b001};
Y = {A, B[0], C[1]};
```

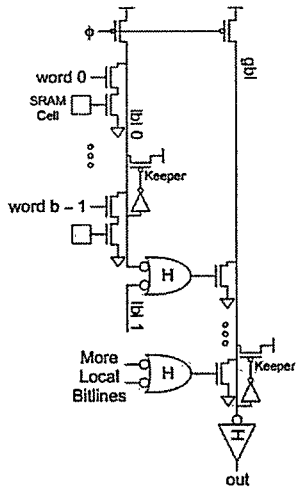
6
b) What are the two methods with which ports are connected to external signals. Explain with help of examples. 6
c) Implement full adder using gate level modelling in Verilog. 6

Q5 a) What are WHILE loop and FOR loop in Verilog? When are they used? Explain their syntax. 6
b) Discuss behavioral modelling in Verilog with help of an example. 6
c) What are nets, registers and vectors in Verilog. What are keywords used for theses 3 data types, explain with examples. 6

Q6 a) Draw the diagram of a 6T full CMOS SRAM cell. What are the ratio constraints that a 6

6T full CMOS SRAM cell should follow to ensure both read stability and writability? Explain.

b) What is the significance of hierarchical bitlines for large signal sensing in 6T Full CMOS SRAM architecture? Identify the diagram below and explain various parts of it.



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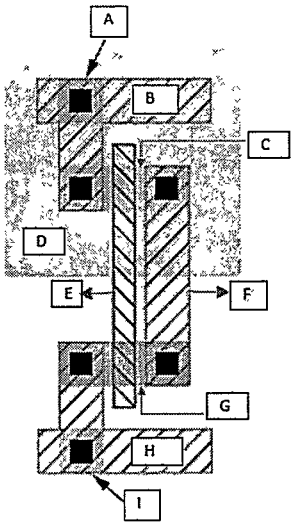
c) Compare and contrast SRAM with DRAM (3 points). Draw the circuit of 1T DRAM cell and explain its working. 6

Q7 a) Describe the role of multiple metal layers in CMOS layouts. Why are higher-level metals typically thicker and wider? Identify the regions labelled in the diagram.



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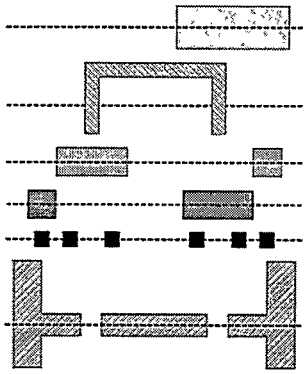
b) Compare full-custom layout design with semi-custom design 6

c)



Identify the 6 mask sequences for a n-well CMOS inverter. Draw and explain the cross-sectional view of a CMOS inverter cell. Highlight the placement of NMOS and PMOS transistors. 6