[This question paper contains 2 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 5327 **J**

Unique Paper Code : 2514001201

Name of the Paper : Digital System Design

Name of the Course : **B.Sc. (H) ELECTRONICS (GE)**

Semester : II

Duration : 3 Hours Maximum Marks : 90

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. There are **seven** questions in all, out of which you have to attempt any **five** questions.
3. **All** questions carry equal marks.
4. **First** Question is Compulsory.

1. (a) Write down Gray code for $(14)_{10}$. (3)

   (b) Draw the symbol for XOR gate and write down truth table for the same. (3)

   (c) What is BCD code? Give example. (3)

   (d) What are combinational logic circuits? (3)

   (e) Draw the circuit of a Half Adder. (3)

   (f) Give the truth table for a SR Flip Flop. (3)

2. (a) Convert $(247.6875)_{10}$ into its octal equivalent number. Then convert the obtained octal number to its hexadecimal equivalent. (9)

   (b) Write down the negative decimal number $(-7)_{10}$ in Sign-magnitude, 1's complement and 2's complement binary representation using four bits. (6)

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(c) What is the only set of inputs that will generate LOW output for a 3 input OR gate? (3)

3. (a) Prove the Boolean theorem AB + A'C = (A + C)(A' + B) using truth table. (8)

(b) Explain the n-input logical AND operation, draw its symbol and write down equation for the same. (5)

(c) Realize AND and OR gates using NAND gates. (5)

4. (a) Realize the following logic equation using logic gates. (9)

$Y = (A'B + BC)(B + C)'$

(b) Simplify the Boolean function $F(x,y,z) = \Sigma m(0,2,4,5,6)$ using K-Map and realize the same using NAND gates. (9)

5. (a) Draw the labelled circuit for a 4-bit parallel Adder. (5)

(b) Give the block diagram of a 1:4 Demultiplexer and explain. (4)

(c) Write down VHDL program for a 3-to-8 line decoder. (9)

6. (a) Implement the following expression using a 8:1 Multiplexer. 10

$F(w,x,y,z) = \Sigma m(0,2,3,6, 8,9,12,14)$

(b) Draw the circuit diagram and the timing diagram of a 3-bit Ring Counter. (8)

7. (a) Give the circuit diagram of SR Flip Flop. Convert it into a D Flip Flop. (6)

(b) Draw the circuit of a 3-bit asynchronous UP counter using JK Flip Flops. Give the timing diagram as well. (9)

(c) How can the a 3-bit asynchronous UP counter using JK Flip Flops be converted to DOWN counter. (3)