[This question paper contains 2 printed pages.]

Your Roll No.....

Sr. No. of Question Paper : 5797 **J**

Unique Paper Code : 2512011202

Name of the Paper : Digital Electronics

Name of the Course : **B.Sc. (H) Electronics**

Semester : II

Duration : 3 Hours Maximum Marks : 90

Instructions for Candidates

1. Write your Roll No. on the top immediately on receipt of this question paper.
2. There are **seven** questions in all, out of which you have to attempt any **five** questions.
3. **All** questions carry equal marks.
4. Sub-parts can be given.
5. **First** Question is Compulsory.

1. (a) Add -75 to +26 using the 8-bit 2's compliment arithmetic.
   (b) Convert $(527)_8$ to Gray code.
   (c) Draw a logic diagram constructing a 3 x 8 decoder with active low enable, using a pair of 2 x 4 decoders.
   (d) Show that characteristic equation for the compliment output of a *JK* flip-flop is $Q'(t+1) = J'Q' + KQ$
   (e) Construct a 2-bit binary ripple counter using *JK* flip-flops.
   (f) Compare TTL logic families with the CMOS logic families. 3x6

2. (a) Express the Boolean function $F = AB + A'C$ in a product of maxterm form. (6)
   (b) State DeMorgan's theorems. Given $(AB)' + A'B = C$. Find $(AC)' + A'C$ with minimum number of literals. (5)
   (c) A 7-bit encoded hamming code (0111001) message is transmitted through noisy channels. Decode the message and find out the error code assuming even parity. (4)
   (d) Convert the hexadecimal number DB4F to binary and then to octal. (3)

3. (a) Design an excess-3-to-BCD code converter. (7)
   (b) Simplify the following expression to (i) sum-of –products and (ii) product-of-sums: (6)
   $x'z' + y'z' + yz' + xy$
   (c) Implement the following function using 8 X 1 multiplexer. (5)

   $F(A,B,C,D) = \Sigma(1,3,4,11,12,13,14,15)$

P.T.O.

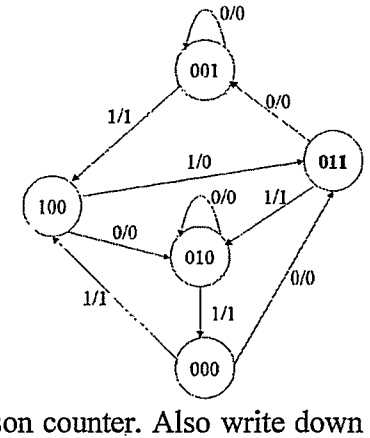
4. (a) Find the minimal expression, using tabulation method, for (8)
$F = \sum m(0,1,6,7,8,9,13,14,15)$

(b) With the help of a block diagram, explain the working of a BCD adder. (6)

(c) Design a 2-to-4 line decoder with enable using NAND and NOT gates. Obtain its truth table. (4)

5. (a) How can a D flip-flop be converted into an SR flip-flop? Provide the conversion table and the logic diagram for this transformation. (7)

(b) A sequential circuit has three flip-flops A, B, C; one input x; and one output, y. The state diagram is shown in Figure below. Design its circuit using D flip-flops. (7)



(c) Construct a 3-bit Johnson counter. Also write down the flip-flop outputs in a sequence. (4)

6. (a) Explain the working principle of a Successive Approximation DAC. How does it convert a digital input to an analog output? (8)

(b) Implement the following two Boolean functions with a PLA: (6)
$F_1(A, B, C) = \Sigma m(0, 1, 2, 4)$
$F_2(A, B, C) = \Sigma m(0, 5, 6, 7)$

(c) Discuss the concepts of fan-in and fan-out in digital circuits. How noise margin affects the performance of logic families in real-world applications. (4)

7 (a) With the help of a circuit diagram, explain the working of a 4-bit universal shift register. (8)

(b) Using D flip-flop, design a counter with the following repeated binary sequence: (7)

0, 1, 2, 4, 6.

Check if it is self-correcting.

(c) Distinguish between SRAMs and DRAMS. (3)

(1000)